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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/663,572	09/15/2003	Philip Yeung	9797-0139-999	2981

38426 7590 02/07/2005

MORGAN LEWIS & BOCKIUS LLP/RAMBUS INC.
2 PALO ALTO SQUARE
3000 EL CAMINO REAL
PALO ALTO, CA 94306

EXAMINER	
WALLING, MEAGAN S	

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 02/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/663,572	YEUNG, PHILIP	
	Examiner	Art Unit	
	Meagan S Walling	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,12,18-20,28-30 and 32* is/are rejected.

7)☒ Claim(s) *11, 13-17, 21-27, and 31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/18/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-7, 18-20, 28-30 and 32 are rejected under 35 U.S.C. 102(e) as being anticipated by Nejedlo et al. (US 2004/0117709).

Regarding claim 1, Nejedlo et al. teaches loading a first pattern into a controller pattern buffer of a controller (see par. 28); transmitting the first pattern to a component of the components (see par. 31); capturing the transmitted first pattern in a component capture buffer of the component (see par. 32); performing a first comparison to compare the captured first pattern to the first pattern (see par. 34); and identifying any interconnect faults based on the first comparison (see par. 34).

Regarding claim 2, Nejedlo et al. teaches preparing the component capture buffer to capture the transmitted first pattern (see par. 29).

Regardign claim 3, Nejedlo et al. teaches placing the component in an interconnect test mode (see par. 29).

Regarding claim 4, Nejedlo et al. teaches that the component is a memory device (see par. 29).

Regarding claim 5, Nejedlo et al. teaches transferring the captured first pattern from the component capture buffer to the controller (see par. 32).

Regarding claim 6, Nejedlo et al. teaches that the captured first pattern is performed via a serial link (see par. 42).

Regarding claim 7, Nejedlo et al. teaches that transmitting the first pattern is performed via a control bus (see par. 32).

Regarding claim 18, Nejedlo et al. teaches a first component (200) comprises first core circuitry, first interface circuitry, and a first communication path (207) coupling the first core circuitry to the first interface circuitry (see par. 29); and a second component (300) comprising second core circuitry, second interface circuitry, and second path (330) coupling the second core circuitry to the second interface circuitry, and interconnect circuitry (250) coupling the first component to the second component, wherein a capture buffer (305) is coupled to the first communication path.

Regarding claim 19, Nejedlo et al. teaches that a second capture buffer (325) is coupled to the second communication path.

Regarding claim 20, Nejedlo et al. teaches that the first communication path comprises a first transmit path and a first receive path, wherein the first capture buffer comprises a first transmit capture buffer (220) coupled to the first transmit communication path and a first receive buffer (305) coupled to the first receive communication path.

Regarding claim 28, Nejedlo et al. teaches a memory controller (122); and a memory device (124) coupled to the memory controller, wherein the memory controller comprises core

circuitry, interface circuitry, and a communication path (207) coupling the core circuitry to the interface circuitry, wherein a capture buffer (305) is coupled to the communication path.

Regarding claim 29, Nejedlo et al. teaches that the communication path comprises a transmit communication path and a receive communication path, wherein the capture buffer comprises a transmit capture buffer (220) coupled to the transmit communication path and a receive capture buffer (305) coupled to the receive communication path.

Regarding claim 30, Nejedlo et al. teaches that the transmit communication path comprises a multiplexer (210) configured to select between a first input coupled to the core circuitry and a second input coupled to a pattern buffer (205).

Regarding claim 32, Nejedlo et al. teaches a first component (200) comprising first core circuitry first interface circuitry, and a first communication means (207) for coupling the first core circuitry to the first interface circuitry (see par. 29); and a second component (300) comprising second core circuitry second interface circuitry, and a second communication means (330) for coupling the core circuitry to the interface circuitry, and interconnection means (250) for coupling the first component to the second component, wherein a means for capturing a test pattern received from the first component is coupled to the last communication means (350).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 8-10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nejedlo et al. in view of Ikeda et al. (US 6,208,571).

Regarding claim 9, Nejedlo et al. teaches performing the memory read operation via a control bus (see par. 32).

Nejedlo et al. teaches all the limitations of claims 8, 10, and 12 except the limitation of loading a second pattern into the memory device via serial link; performing a memory read operation; capturing the second pattern received from the memory device; performing a second comparison to compare the captured second pattern to the second pattern; and identifying any interconnect faults based on the second comparison (current claim 8) and that the step of capturing the second pattern is performed by capturing the second pattern received from the memory device via a data bus (current claim 10) and that the second pattern is identical to the first (current claim 12)..

Regarding claim 8, Ikeda et al. teaches outputting second output patterns generated from the pattern generating circuit and performing an interconnection test to determine if any faults exist (see paragraph 8, lines 44-49).

Regarding claim 10, Ikeda et al. teaches that the step of capturing the second pattern is performed by capturing the second pattern received from the memory device via a data bus (column 11, lines 50-51).

Regarding claim 12, Ikeda et al. teaches that the second pattern is identical to the first (column 8, lines 55-56).

It would have been obvious to one skilled in the art at the time of the invention to combine the teachings of Nejedlo et al. with the teachings of Ikeda et al. to perform the

interconnection test on a second pattern. The motivation for making this combination would be to test more than one interconnection to see if there was a fault in a different location.

Allowable Subject Matter

Claims 11, 13-17, 21-27 and 31 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The primary reason for the indication of allowability of claim 11 is the inclusion of the limitation of loading the second pattern into the controller pattern buffer of the controller. It is this limitation in the claimed combination that has not been found, taught, or suggested by the prior art of record that makes these claims allowable.

The primary reason for the indication of allowability of claim 13 is the inclusion of the limitation of loading a second pattern into a component pattern buffer of the component; transmitting the second pattern to the controller; capturing the transmitted second pattern in a controller capture buffer of the controller; and performing a second comparison to compare the captured second pattern to the second pattern, wherein the step of identifying any interconnect faults is based on the first comparison and the second comparison. It is this limitation in the claimed combination that has not been found, taught, or suggested by the prior art of record that makes these claims allowable.

The primary reason for the indication of allowability of claim 21 is the inclusion of the limitation that the second communication path further comprises a second transmit

communication path and a second receive communication path, wherein the second capture buffer further comprises a second transmit capture buffer coupled to the second transmit communication path and a second receive capture buffer coupled to the second receive communication path. It is this limitation in the claimed combination that has not been found, taught, or suggested by the prior art of record that makes these claims allowable.

The primary reason for the indication of allowability of claim 31 is the inclusion of the limitation that the memory device is coupled to the memory controller via a memory serial link, a control bus, and a data bus. It is this limitation in the claimed combination that has not been found, taught, or suggested by the prior art of record that makes these claims allowable.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Meagan S Walling whose telephone number is (571) 272-2283. The examiner can normally be reached on Monday through Friday 8:30 AM to 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on (571) 272-2269. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

msw

John Barlow
Supervisory Patent Examiner
Technology Center 2800